Arria 10 DDR4 IP Parameterization

Selecting the DDR4 IP timing parameters from a Micron DDR4 device data sheet :

Memory Topology and Memory Timing tabs

Presets

- ◖ **Based on JEDEC specifications**
- ◖ **Use as a starting point**
  - – Select a preset close to the requirement
    - ◖ Memory Format
      - – Discrete Device
      - – DIMM (UDIMM, RDIMM, LRDIMM)
    - ◖ Configuration
      - – Maximum Throughput (DDR4-xxxx)
      - – CAS latency
      - – Rank/chip select
      - – Capacity
      - – Device Width
- ◖ **Then modify as required**
  - – Some memory timing parameters may need to be changed

- ◖ **DDR4 DIMMS**
  - – To find the actual memory device used on the DIMM
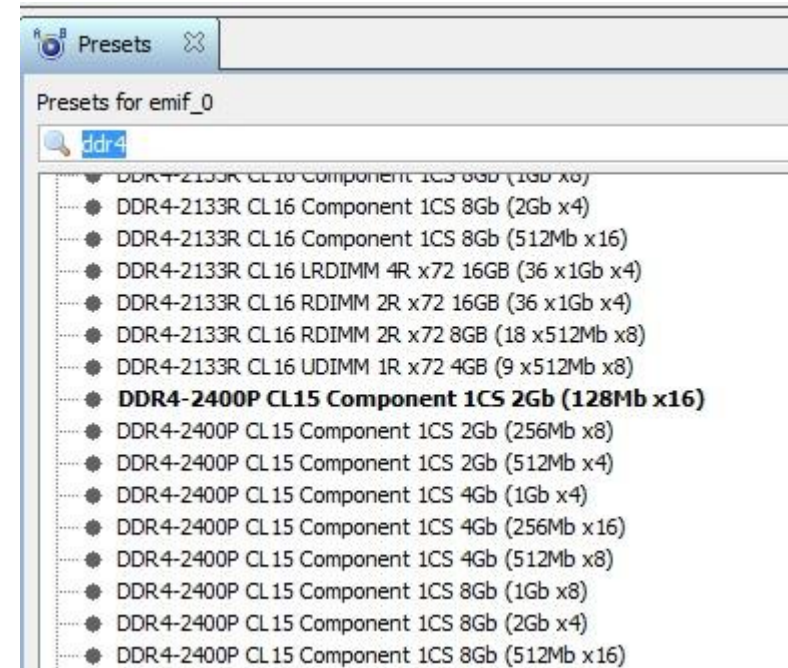   - ◖ Get the Base device part number from the DIMM datasheet

Presets ⊠

Presets for emif_0

🔍 ddr4

- ● DDR4-2133R CL16 Component 1CS 8Gb (1Gb x8)
- ● DDR4-2133R CL16 Component 1CS 8Gb (2Gb x4)
- ● DDR4-2133R CL16 Component 1CS 8Gb (512Mb x16)
- ● DDR4-2133R CL16 LRDIMM 4R x72 16GB (36 x1Gb x4)
- ● DDR4-2133R CL16 RDIMM 2R x72 16GB (36 x1Gb x4)
- ● DDR4-2133R CL16 RDIMM 2R x72 8GB (18 x512Mb x8)
- ● DDR4-2133R CL16 UDIMM 1R x72 4GB (9 x512Mb x8)
- ● **DDR4-2400P CL15 Component 1CS 2Gb (128Mb x16)**
- ● DDR4-2400P CL15 Component 1CS 2Gb (256Mb x8)
- ● DDR4-2400P CL15 Component 1CS 2Gb (512Mb x4)
- ● DDR4-2400P CL15 Component 1CS 4Gb (1Gb x4)
- ● DDR4-2400P CL15 Component 1CS 4Gb (256Mb x16)
- ● DDR4-2400P CL15 Component 1CS 4Gb (512Mb x8)
- ● DDR4-2400P CL15 Component 1CS 8Gb (1Gb x8)
- ● DDR4-2400P CL15 Component 1CS 8Gb (2Gb x4)
- ● DDR4-2400P CL15 Component 1CS 8Gb (512Mb x16)

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT40A512M8,[1] 4Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Mod Bandw
MTA8ATF51264AZ-2G3__	4GB	512 Meg x 64	19.2 (

ALTERA

Memory Timing 1

◄ Memory device Speed bin defines the maximum data rate that the memory device can support

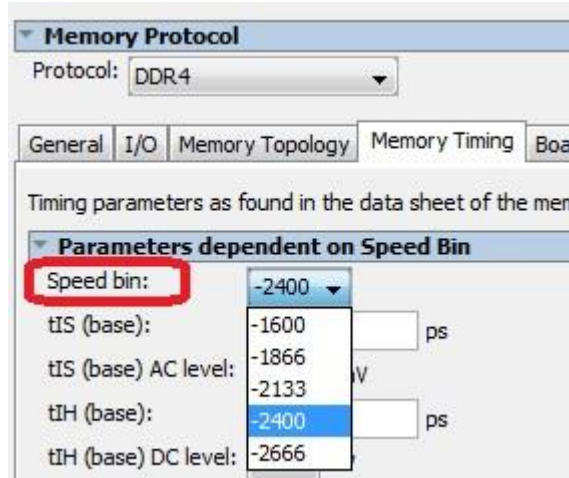– Get from the DDR4 memory device part number speed grade

Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	
-083E[1, 2, 3, 4]	2400	
-093F[1, 2, 3]	2133	
-093E[1, 2]	2133	
-107E[1]	1866	

– Speed grade may have a letter suffix
  ◄ Indicates CAS latency, tRCD, tRP

Memory Topology 1

◖ Memory Topology -> Mode Register Settings : Latencies

◖ -> Use Memory Device data sheet Speed bin table

– Take into account

◖ Memory speed grade

◖ DDR4 clock period tCK

◖ DBI

Table 139: DDR4-2400 Speed Bins and Operating Conditions

DDR4-2400 Speed Bin				-083F		-083E		-083		
CL-*n*RCD-*n*RP				15-15-15		16-16-16		17-17-17		
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data			^tAA	12.5	18.00	13.32	18.00	14.16	18.00	ns

READ: nonDBI	READ: DBI	WRITE	Symbol	Min`	Max	Min	Max	Min	Max	Unit
CL = 9	CL = 11	CWL = 9	^tCK	1.5	1.6	1.5	1.6	Reserved		ns
CL = 10	CL = 12	CWL = 9	^tCK	1.5	1.6	Reserved		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^tCK	Reserved		Reserved		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^tCK	Reserved		1.25	<1.5	1.25	<1.5	ns
CL = 12	CL = 14	CWL = 9, 11	^tCK	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns
CL = 12	CL = 14	CWL = 10, 12	^tCK	Reserved		Reserved		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^tCK	Reserved		1.071	<1.25	1.071	<1.25	ns
CL = 14	CL = 16	CWL = 10, 12	^tCK	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns
CL = 14	CL =17	CWL = 11, 14	^tCK	Reserved		Reserved		Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	^tCK	Reserved		0.937^6	<1.071	0.937	<1.071	ns
CL = 16	CL = 19	CWL = 11, 14	^tCK	0.937	<1.071	0.937	<1.071	0.937	<1.071	ns
CL = 15	CL = 18	CWL = 12, 16	^tCK	0.833	<0.937	Reserved		Reserved		ns
CL = 16	CL = 19	CWL = 12, 16	^tCK	0.833	<0.937	0.833	<0.937	Reserved		ns
CL = 17	CL = 20	CWL = 12, 16	^tCK	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
CL = 18	CL = 21	CWL = 12, 16	^tCK	0.833	<0.937	0.833	<0.937	0.833	<0.937	ns
Supported CL settings				9, 10, 12, 14–18		9, 11–18		10–18		nCK
Supported CL settings with read DBI				11, 12, 14, 16–21		13–16, 18–21		12–16, 18–21		nCK
Supported CWL settings				9, 10, 11, 12, 14, 16		9, 10, 11, 12, 14, 16		9, 10, 11, 12, 14, 16		nCK

Memory Timing 2

◖ Presets are typically for the DDR4 device speed grade **clocked at its highest frequency**

◖ **Some parameters may need to be modified :**

- – Clocking at lower frequency
- – Using an industrial temperature DDR4 device
  - ◖ Refesh rate tREFI -> 3.9us

General	I/O	Memory Topology	Memory Timing	Board Timing	Controller	Diagnostics

Timing parameters as found in the data sheet of the memory device.

▼ Parameters dependent on Speed Bin

Parameter	Value	Unit
Speed bin:	-2400 ▾	
tIS (base):	60	ps
tIS (base) AC level:	100 ▾	mV
tIH (base):	95	ps
tIH (base) DC level:	75 ▾	mV
tdIVW_dj:	0.1	cycles
VdiVW_total:	136	mV
tDQSQ:	66	ps
tQH:	0.38	cycles
tDQSCK:	165	ps
tDQSS:	0.27	cycles
tQSH:	0.38	cycles
tDSH:	0.18	cycles
tDSS:	0.18	cycles
tWLS:	108.0	ps
tWLH:	108.0	ps
tINIT:	500	us
tMRD:	8	cycles
tRAS:	32.0	ns
tRCD:	12.5	ns
tRP:	12.5	ns
tWR:	15.0	ns

▼ Parameters dependent on Speed Bin, Operating Frequency, and Page Size

Update the following as you change the operating frequency, even if the device speed bin has not changed.

Parameter	Value	Unit
tRRD_S:	7	cycles
tRRD_L:	8	cycles
tFAW:	30.0	ns
tCCD_S:	4	cycles
tCCD_L:	6 ▾	cycles
tWTR_S:	3	cycles
tWTR_L:	9	cycles

▼ Parameters dependent on Density and Temperature

Update the following as you change the physical memory device density.
Incorrect values can cause data corruption.

Parameter	Value	Unit
tRFC:	160.0	ns
tREFI:	7.8	us

Memory Timing 3

- From the Electrical Characteristics and AC Timing Parameters table
  - Use the DDR4-xxxx column
    that the device is rated for
    - eg 1200MHz device -> use DDR4-2400

- From the Electrical Characteristics and AC Timing Parameters table
  - Use the DDR4-xxxx column that the device is rated for
  - Calculate values as required using :
    - Page size (0.5K, 1K or 2K)
    - Memory Clock Frequency (tCK)

- See next slide for data sheet extracts

Memory Timing 4

◄ Extracts from a Micron Memory DDR4 Datasheet

Table 2: Addressing

Parameter	1024 Meg x 4	512 Meg x 8	256 Meg x 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	64K (A[15:0])	32K (A[14:0])	32K (A[14:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B / 1KB[2]	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:
          Page size = $2^{COLBITS}$ × ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

Table 143: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
DLL locking time		^tDLLK	597	–	597	–	768	–	768	–	CK
CMD, ADDR setup time to CK_t, CK_c referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^tIS	115	–	100	–	80	–	62	–	ps
	V_{REFCA}	$^tIS_{VREF}$	215	–	200	–	180	–	162	–	ps
CMD, ADDR hold time to CK_t, CK_c referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^tIH	140	–	125	–	105	–	87	–	ps
	V_{REFCA}	$^tIH_{VREF}$	215	–	200	–	180	–	162	–	ps
CTRL, ADDR pulse width for each input		^tIPW	600	–	525	–	460	–	410	–	ps
ACTIVATE to internal READ or WRITE delay		^tRCD	See Speed Bin Tables for ^tRCD								ns
PRECHARGE command period		^tRP	See Speed Bin Tables for ^tRP								ns
ACTIVATE-to-PRECHARGE command period		^tRAS	See Speed Bin Tables for ^tRAS								ns
ACTIVATE-to-ACTIVATE or REF command period		^tRC	See Speed Bin Tables for ^tRC								ns
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size		$^tRRD\_S$ (1/2KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size		$^tRRD\_S$ (1KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size		$^tRRD\_S$ (2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		CK
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size		$^tRRD\_L$ (1/2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size		$^tRRD\_L$ (1KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size		$^tRRD\_L$ (2KB)	MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		CK
Four ACTIVATE windows for 1/2KB page size		^tFAW (1/2KB)	MIN = greater of 16CK or 20ns		MIN = greater of 16CK or 17ns		MIN = greater of 16CK or 15ns		MIN = greater of 16CK or 13ns		ns

Memory Timing 5

◄ From the Command and Address Input Levels table

◄ From the DQ Input Receiver Specifications table

◄ From the Reset and Initialization description

◄ From the Speed Bins and Operating Conditions table

◄ See next slide for data sheet extracts

◄ Extracts from a Micron Memory DDR4 Datasheet

Table 80: Command and Address Input Levels: DDR4-1600 Through DDR4-2400

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	$V_{REF} + 100$	$V_{DD}5$	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	$V_{REF} + 75$	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	$V_{REF} - 75$	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	$V_{SS}5$	$V_{REF} - 100$	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	$0.49 \times V_{DD}$	$0.49 \times V_{DD}$	V	4

Table 82: DQ Input Receiver Specifications

Note 1 applies to the entire table

Parameter	Symbol	DDR4-1600, 1866, 2133 Min	Max	DDR4-2400 Min	Max	DDR4-2666, 3200 Min	Max	Unit	Notes
V_{IN} Rx mask input peak-to-peak	V_{dIVW}	–	136[1]	–	130[1]	–	125	mV	2, 3
DQ Rx input timing window	TdIVW	–	0.2[1]	–	0.2[1]	–	0.22[1]	UI	2, 3
DQ AC input swing peak-to-peak	$V_{IHL(AC)}$	186	–	160	–	150	–	mV	4, 5
DQ input pulse width	TdIPW	0.58	–	0.58	–	0.58	–	UI	6
DOS-to-DO Rx mask offset	$^tDOS2DO$	–0.17	0.17	–0.17	0.17	–0.22	0.22	UI	7

Table 139: DDR4-2400 Speed Bins and Operating Conditions

DDR4-2400 Speed Bin				-083F		-083E		-083		
CL-nRCD-nRP				15-15-15		16-16-16		17-17-17		
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data		^tAA		12.5	18.00	13.32	18.00	14.16	18.00	ns
Internal READ command to first data with read DBI enabled		^tAA_DBI		$^tAA(MIN) + 3nCK$	–	$^tAA(MIN) + 3nCK$	–	$^tAA(MIN) + 3nCK$	–	ns
ACTIVATE to internal READ or WRITE delay time		^tRCD		12.5	–	13.32	–	14.16	–	ns
PRECHARGE command period		^tRP		12.5	–	13.32	–	14.16	–	ns
ACTIVATE-to-PRECHARGE command period		^tRAS		32	$9 \times {}^tREFI$	32	$9 \times {}^tREFI$	32	$9 \times {}^tREFI$	ns
ACTIVATE-to-ACTIVATE or REFRESH command period		^tRC		$^tRAS + {}^tRP$	–	$^tRAS + {}^tRP$	–	$^tRAS + {}^tRP$	–	ns
READ: nonDBI	READ: DBI	WRITE	Symbol	Min	Max	Min	Max	Min	Max	Unit
CL = 9	CL = 11	CWL = 9	^tCK	1.5	1.6	1.5	1.6	Reserved		ns
CL = 10	CL = 12	CWL = 9	^tCK	1.5	1.6	Reserved		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^tCK	Reserved		Reserved		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^tCK	Reserved		1.25	<1.5	1.25	<1.5	ns
CL = 12	CL = 14	CWL = 9, 11	^tCK	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns

Power-Up and Initialization Sequence

2. After RESET_n is de-asserted, wait for another 500µs until CKE becomes active.

Memory Timing 7

◄ Check tRFC is correct for the capacity of the DDR4 memory device
  – Use the tRFC1 value from the DDR4 datasheet

Refresh Timing				
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	$^tRFC1$	MIN = 260	ns
		$^tRFC2$	MIN = 160	ns
		$^tRFC4$	MIN = 110	ns
	8Gb	$^tRFC1$	MIN = 350	ns
		$^tRFC2$	MIN = 260	ns
		$^tRFC4$	MIN = 160	ns
	16Gb	$^tRFC1$	MIN = 550	ns
		$^tRFC2$	MIN = 405	ns
		$^tRFC4$	MIN = 250	ns
Average periodic re-fresh interval	$0°C \leq T_C \leq 85°C$	^tREFI	MIN = N/A; MAX = 7.8	μs
	$85°C < T_C \leq 95°C$	^tREFI	MIN = N/A; MAX = 3.9	μs

◄ Using the incorrect value can cause bit errors during memory accesses

Memory Timing 8

◀ Some timing parameters are in units of UI or UId
  – UI/UId is defined as the Unit Interval
  – Jedec specification formula : UI = minimum [tCK(avg)/2]
  – For the DDR4 IP parameters, set UI = tCK/2

Table 143: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
DQ Output Timing										
DQS_t, DQS_c to DQ skew, per group, per access	^{t}DQSQ	–	0.16	–	0.16	–	0.16	–	0.17	UI_d
DQ output hold time from DQS_t, DQS_c	^{t}QH	0.76	–	0.76	–	0.76	–	0.74	–	UI_d