

Exploiting the
modularity of
pipeline FFTs
for reusable
design

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Outline

Overview

Radix2 : Multi
Delay Feedback

Radix2 : Single
Delay Feedback

Butterfly(BF)

BF Stage

R2SDF Stage

Twiddles

Big picture

Conclusion and
Discussion

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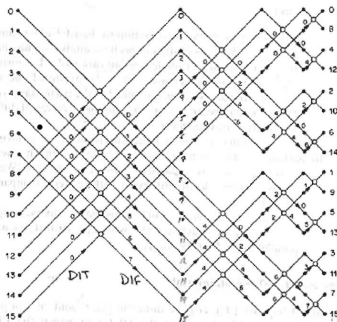


Fig. 10.1 In-place 16-point FFT with normally ordered inputs and bit-reversed outputs.

Discrete Fourier Transform

- given $\{x(n)\}$:

$$X(k) = \sum_{n=0}^N x(n)W^{nk}$$

$$\dots 0 \leq n, k \leq N-1$$
- N^2 multiplications !

Fast Fourier Transform

- periodic nature of Twiddles : W^{nk}
- Classical Parallel : $\frac{N}{2} \times \log_p N$
- Radix-2, Radix-4, Multi Radix architectures
- Alternative \rightarrow Pipeline architecture

R2MDF

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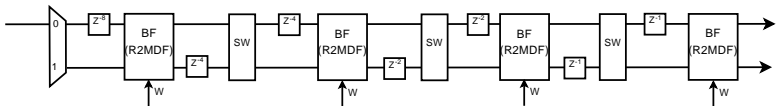


Figure: R2MDF: N=16

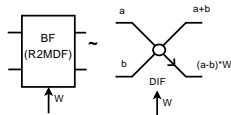
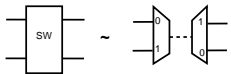


Figure: R2MDF: N=16 : Butterfly and Switch

■ #Multipliers : $2(\log_4 N - 1)$, #Memory : $3\frac{N}{2} - 2$

R2SDF

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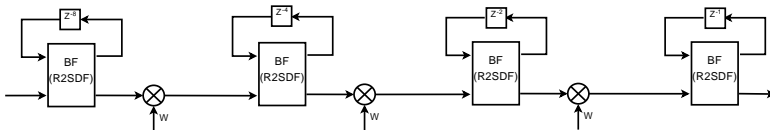


Figure: R2SDF: N=16

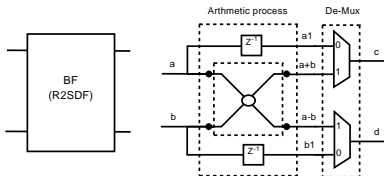


Figure: R2MDF: N=16 : Butterfly

■ #Multipliers : $2(\log_4 N - 1)$, #Memory : $N - 1$

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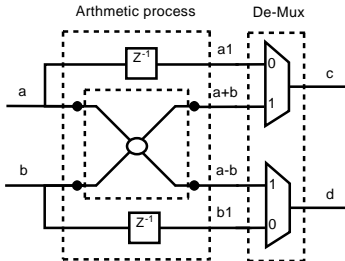
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Butterfly behaviour

```
--  
prcCntrl:  
process(clk,rstH)  
begin  
  -- ...control, sync and delay  
end process prcCntrl;  
  -- rad Two Cross  
cmpRadTwoCross: rTwoCross  
generic map(Nb)  
port map(clk, rstH, a, b, aPb, aMb);  
  --SW: De-mux  
cmpDeMuxC: deMux21  
port map (clk, rstH, '1', sel1, a1, aPb, c);  
cmpDeMuxD: deMux21  
port map (clk, rstH, '1', sel1, b1, aMb, d);  
--
```

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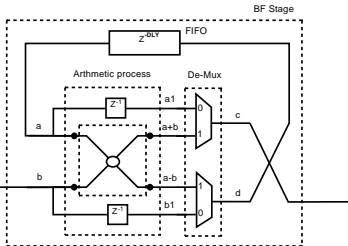
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BF Stage behaviour

-- *butterfly stage*

cmpRTwoBf: rTwoBF

generic map(Nb)

port map(clk, rstH, synIn, sel, a, b, c, d, syn);

--

-- *feedback fifo*

cmpfifo: fifo

generic map(c'length, pow2(r-1))

port map(clk, rstH, syn, d, a);

--

R2SDF Stage

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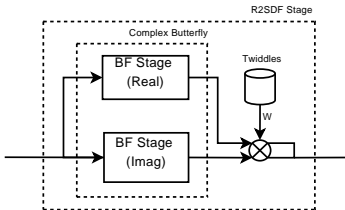
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BF Cmplx Stage behaviour

-- *butterfly Real*

butterflyRe: rTwoBFStage

generic map(inRe'length,r)

port map (clk,rstH,synIn,sel,inRe,outRe,syn(1));

--

-- *butterfly Imaginary*

butterflyIm: rTwoBFStage

generic map(inRe'length,r)

port map (clk,rstH,synIn,sel,inRe,outRe,syn(2));

--

synOut <= syn(1);

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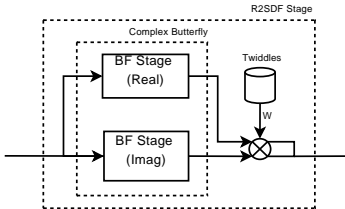
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- Twiddles generator
- `twiddles.m` → `twiddlesPkg.vhd`
- Inputs : Nbits, Npoint.
- Outputs : WRe, WIm, W Map (for specific architecture)
- pure MATLAB/Octave code, No Simulink

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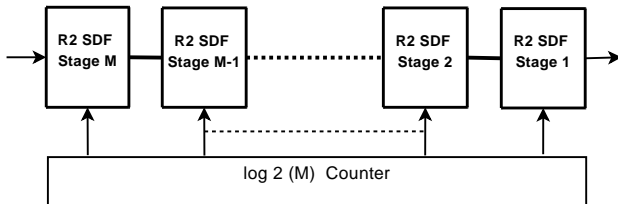


Figure: R2SDF: N point, $M = \log_2(N)$ Stages

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■ Current Status

FFT : R2SDF coding is complete

Library : FIFO, Cmplx Arithmetic, Mux, De-Mux
: tested, ready and synthesisable

■ Next Steps

FFT : R2SDF Testing using LOFAR VHDL testbenchs.

Library : consolidate components for re-use

■ Discussion...